This listing of claims replaces all prior versions, and listings of claims in the instant application:

Listing of Claims:

1-24. (Canceled)

25. (Currently amended) A stackable semiconductor package comprising:

a substrate having a first surface, an opposite second surface, and central throughhole between the first and second surfaces;

a plurality of electrically conductive circuit patterns on each of the first and second surfaces of the substrate, wherein the circuit patterns of each of the first and second surfaces of the substrate include a plurality of lands, the circuit patterns of the first surface also include a plurality of bond fingers, and at least some of the circuit patterns of the first surface are electrically connected through the substrate to some of the circuit patterns of the second surface;

a semiconductor chip in said throughhole and electrically connected to the bond fingers, wherein the semiconductor chip has a first surface with bond pads thereon, and an opposite second surface, the first surface of the semiconductor chip faces in a same direction as the first surface of the substrate, and the second surface of the semiconductor chip is flush with the second surface of the substrate, wherein the second surface of the semiconductor chip is exposed; and

a hardened encapsulant within said through hole and covering the semiconductor chip and the bond fingers, wherein the lands of each of the first and second surfaces are outward of a perimeter of the encapsulant.

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26. (Previously presented) The stackable semiconductor package of claim 25, wherein the substrate further comprises a cover coat over the circuit patterns of the first and second surfaces of the substrate, wherein the respective lands and bond fingers are exposed through respective apertures in the cover coat.

27. (Previously presented) The stackable semiconductor package of claim 25, further comprising a plurality of electrically conductive balls, wherein each of the conductive balls is fused to a respective one of the lands of the first surface of the substrate.

28. (Previously presented) The stackable semiconductor package of claim 27, further comprising a plurality of second electrically conductive balls, wherein each of the second electrically conductive balls is fused to a respective one of the lands of the second surface of the substrate.

29. (Previously presented) The stackable semiconductor package of claim 25, further comprising a plurality of electrically conductive balls, wherein some of said electrically conductive balls are fused to respective ones of the lands of the first surface of the substrate and some of said electrically conductive balls are fused to respective ones of the lands of the second surface of the substrate.

30. (Previously presented) The stackable semiconductor package of claim 25, further comprising a plurality of electrically conductive balls, wherein each said electrically conductive ball is fused to a respective one of the lands of the second surface of the substrate.

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31. (Currently amended) A stack of semiconductor packages comprising:

a first semiconductor package comprising: (a) a substrate having a first surface, an opposite second surface, and central throughhole between the first and second surfaces; (b) a plurality of electrically conductive circuit patterns on each of the first and second surfaces of the substrate, wherein the circuit patterns of each of the first and second surfaces of the substrate include a plurality of lands, the circuit patterns of the first surface also include a plurality of bond fingers, and at least some of the circuit patterns of the first surface are electrically connected through the substrate to some of the circuit patterns of the second surface that include respective ones of the lands; (c) a semiconductor chip in said throughhole and electrically connected to the bond fingers, wherein the semiconductor chip has a first surface with bond pads thereon, and an opposite second surface, the first surface of the semiconductor chip faces in a same direction as the first surface of the substrate, and the second surface of the semiconductor chip is flush with the second surface of the substrate, wherein the second surface of the semiconductor chip is exposed; (d) a hardened encapsulant within said through hole and covering the semiconductor chip and the bond fingers, wherein the lands of each of the first and second surfaces are outward of a perimeter of the encapsulant; and (e) a plurality of electrically conductive balls, wherein each of the conductive balls is fused to a respective one of the lands of the first surface of the substrate; and

a second semiconductor package comprising a plurality of second electrically conductive balls, wherein the second semiconductor package is in a stack with the first

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semiconductor package, and the second electrically conductive balls of the second package each superimpose and are electrically connected to a respective one of the lands of the second surface of the substrate of the first semiconductor package.

32. (Previously presented) The stack of claim 31, wherein the second semiconductor package includes a second substrate with a central second throughhole, the second semiconductor chip is in the second throughhole, and the second semiconductor package further comprises a hardened second encapsulant in the second throughhole and covering the second semiconductor chip.

33. (Currently amended) The ~~stackable semiconductor package~~ stack of claim 32, wherein the substrate of the first package further comprises a cover coat over the circuit patterns of the first and second surfaces of the substrate, wherein the respective lands and bond fingers are exposed through respective apertures in the cover coat.

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